IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appellants:	Andrej KICEV et al.	§	Confirmation No.:	4863
Serial No.:	10/685,028	§	Group Art Unit:	2116
Filed:	10/14/2003	§	Examiner:	M. J. Brown
For:	Computer System, Carrier Medium And Method For Adjusting An Expiration Period	§	Docket No.:	200208956-1

APPEAL BRIEF

Mail Stop Appeal Brief – Patents
Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

Date: April 13, 2007

Sir:

Appellants hereby submit this Appeal Brief in connection with the above-identified application. A Notice of Appeal was filed via facsimile on February 15, 2007.

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I. REAL PARTY IN INTEREST

The real party in interest is the Hewlett-Packard Development Company (HPDC), a Texas Limited Partnership, having its principal place of business in Houston, Texas. The Assignment from the inventors to HPDC was recorded on October 14, 2003, at Reel/Frame 014612/0977.

II. RELATED APPEALS AND INTERFERENCES

Appellants are unaware of any related appeals or interferences.

III. STATUS OF THE CLAIMS

Originally filed claims:	1-36.
Claim cancellations:	19-36.
Added claims:	None.
Presently pending claims:	1-18.
Presently appealed claims:	1-18.

IV. STATUS OF THE AMENDMENTS

No claims were amended after the Final Office Action dated October 10, 2006.

V. SUMMARY OF THE CLAIMED SUBJECT MATTER

A source device may initiate a read or write data transfer to a target device in an electronic system (e.g., a computer) using a particular protocol (e.g., Peripheral Bus Interconnect (PCI) protocol). Such protocols typically define a time period by which the target device must respond to the transaction from the source. See e.g., para. [0029]. The target device may initiate a "delayed transaction" when, for example, the target device cannot respond in the time required. The target device asserts a signal that causes the source device to try to complete the transaction at a later time. For example, if the source attempts to read data from the target and the target cannot provide the requested data in the allotted time, the source will attempt to complete the read transaction at a later. See e.g., paras. [0030-0031]. However, even delayed transactions must be completed within a protocol-specified time period ("expiration period"). See e.g., para. [0033]. If the transaction undesirably has not been completed by the end of the expiration period (due to a slow source or a slow target), a "time-out signal" is sent to the source and the source stops trying to complete the transaction. Appellants have solved this problem by providing a mechanism that programmably extends the expiration period for a delayed transaction. Figures 2-6 and paras. [0039-0069] discuss the solution.

According to the invention of claim 1, for example, a system comprises a timing logic unit (Fig. 2, 300) to produce a predetermined number of pulses in response to a transaction request transmitted from a source device to a target device. The timing logic unit is configured to generate a time expired signal upon producing a last one of the predetermined number of pulses. The system also comprises a processor (Fig. 1, 110) for executing program instructions configured to programmably alter a rate at which the predetermined number of pulses are produced by the timing logic unit to thereby adjust an expiration period for completing a transaction cycle associated with the transaction request. See e.g. paras. [0008], [0039]-[0068].

According to the invention of claim 8 a computer system (Fig. 1, 100) comprises a source device configured to initiate a transaction cycle by sending a

transaction request to a target device. The system also comprises a timing logic (Fig. 2, 300) unit arranged within the target device. The timing logic unit comprises a time register (Fig. 3, 360) for storing a predetermined expiration value and a first counter for (Fig. 3, 350) receiving a number of pulses corresponding to the predetermined expiration value and generating a time expired signal upon receipt of a last one of the number of pulses. The system also comprises a memory device (Fig. 1, 130) for storing program instructions configured to programmably alter a rate at which the number of pulses are received by the first counter, thereby adjusting an expiration period for completing the transaction cycle. See e.g. paras. [0009], [0039]-[0068].

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Whether claims 1-18 are anticipated by Harrell (U.S. Pat. No. 5,682,554).

VII. ARGUMENT

A. Overview of Harrell

Harrell purports to the solve the problem of a host computer 22 that operates with a clock frequency and that attempts to send data to a graphics processor 21 (Fig. 2) that operates in accordance with a different clock frequency. That is, the host computer may provide data to the graphics processor at a rate that differs from the rate at which the graphics processor can consume the data. See e.g., cols. 1 and 2. Harrell solves this problem by providing an interface 23 between the host computer 22 and graphics processor 21 (Fig. 2). The interface 23 contains a first in first out (FIFO) data buffer 24 and a pair of counters 25 and 26. Data is provided by the host computer on bus 40 and stored in the FIFO buffer. The graphics process extracts the data from the FIFO data buffer via bus 42.

In Harrell, it may be that the graphics processor 21 is unable to retrieve the data from the FIFO data buffer as fast as the host computer 22 is storing data into the FIFO data buffer. In this situation, the FIFO data buffer will become full. On the other hand, it may be that the host computer 22 cannot store data into the FIFO buffer as fast as the graphics controller 21 retrieves the data from the FIFO buffer. In this situation, the FIFO data buffer will become empty. Neither condition is desirable. The counter 25 will cause an interrupt to be generated to the host computer when the FIFO buffer is almost full. This interrupt will cause the host computer to cease storing data into the FIFO buffer. The counter 26 will cause an interrupt to be generated to the graphics controller when the FIFO buffer is almost empty. This interrupt will cause the graphics controller to cease trying to retrieve data from the FIFO buffer.

B. Claims 1-7

Appellants select claim 1 as representative of this claim grouping. Claim 1 requires "a processor for executing program instructions configured to programmably alter a rate at which the predetermined number of pulses are produced by the timing logic unit, thereby adjusting an expiration period for completing a transaction cycle associated with the transaction request." Claim 1

is substantially different than the teachings of Harrell. The Examiner has stated that Harrell's first in first out (FIFO) data buffer is akin to the claimed "processor." Clearly, a FIFO data buffer, which simply stores data, is not the same as a processor that executes program instructions. In the Final Office Action, the Examiner stated that the FIFO buffer receives data and then transfers the data to the graphics processor, and that the data received by the FIFO buffer alters the rate of which the preset value is produced by a counter. According to the examiner, a "FIFO does not simply store data, but also processes that data." Final Office Action pp. 7-8.

Appellants respectfully contend that the Examiner appears to understand a FIFO buffer to be very different from how one of ordinary skill in the art would understand a FIFO buffer to be. One of ordinary skill in the art would understand a FIFO buffer to simply be a repository into which data can be stored and retrieved. In a FIFO buffer, the data read from the buffer is the oldest data resident in the buffer (i.e., the first data written to the buffer). The Examiner somehow contends that a FIFO buffer does more than just store data. Appellants submit that the Examiner's understanding of the operation of a FIFO buffer is counter to what one of ordinary skill in the art would understand.

Claim 1 requires "a processor for executing program instructions configured to programmably alter a rate at which the predetermined number of pulses are produced by the timing logic unit, thereby adjusting an expiration period for completing a transaction cycle associated with the transaction request." By arguing that Harrell's FIFO buffer is akin to the claimed processor, the Examiner contends that the FIFO buffer "executes program instructions." One of ordinary skill in the art would not understand a FIFO buffer to execute program instructions, much less execute program instructions that accomplish what claim 1 requires.

With regard to independent claim 8 (discussed below) which requires a "memory device," the Examiner stated that Harrell's FIFO buffer is the claimed "memory device." The Examiner states that Harrell's FIFO buffer is akin to the processor of claim 1 and also akin to the memory device of claim 8. Thus,

according to the Examiner, a memory device is equivalent to a processor. One of ordinary skill in the art would certainly not believe that to be the case.

Further, Harrell fails to teach or even suggest any type of logic that alters the rate at which a predetermined number of pulses are produced by timing logic to thereby adjust an expiration period. Harrell does not even teach the concept of an "expiration period" as claimed, that is, an expiration period for completing a transaction cycle associated with a transaction request.

For at least these reasons, Appellants contend that the Examiner erred in rejecting claim 1 and its dependent claims. Accordingly, Appellants respectfully submit that the rejections of the claims in this grouping be reversed, and the claims set for issue.

C. Claims 8-18

Appellants select claim 8 as representative of this claim grouping. Claim 8 requires "a memory device for storing program instructions configured to programmably alter a rate at which the number of pulses are received by the first counter, thereby adjusting an expiration period for completing the transaction cycle." The Examiner stated that Harrell's FIFO buffer is the claimed memory device. However, Harrell's FIFO buffer does not store program instructions which themselves programmably alter the "rate at which the number of pulses are received by the first counter, thereby adjusting an expiration period for completing the transaction cycle."

Further, Harrell fails to teach or even suggest altering the rate at which a number of pulses are received by a counter, thereby adjusting an expiration period for completing a transaction cycle. Harrell does not even teach the concept of an "expiration period" as claimed, that is, an expiration period for completing a transaction cycle associated with a transaction request.

For at least these reasons, Appellants contend that the Examiner erred in rejecting claim 8 and its dependent claims. Accordingly, Appellants respectfully submit that the rejections of the claims in this grouping be reversed, and the grouping set for issue.

D. Conclusion

For the reasons stated above, Appellants respectfully submit that the Examiner erred in rejecting all pending claims. It is believed that no extensions of time or fees are required, beyond those that may otherwise be provided for in documents accompanying this paper. However, in the event that additional extensions of time are necessary to allow consideration of this paper, such extensions are hereby petitioned under 37 C.F.R. § 1.136(a), and any fees required (including fees for net addition of claims) are hereby authorized to be charged to Hewlett-Packard Development Company's Deposit Account No. 08-2025.

Respectfully submitted,

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VIII. CLAIMS APPENDIX

1. (Original) A system, comprising:

a timing logic unit coupled to produce a predetermined number of pulses in response to a transaction request transmitted from a source device to a target device, wherein the timing logic unit is configured to generate a time expired signal upon producing a last one of the predetermined number of pulses; and

a processor for executing program instructions configured to programmably alter a rate at which the predetermined number of pulses are produced by the timing logic unit, thereby adjusting an expiration period for completing a transaction cycle associated with the transaction request.

2. (Original) The system as recited in claim 1, wherein the program instructions are configured to programmably decrease the rate for increasing the expiration period.

3. (Original) The system as recited in claim 1, wherein the program instructions are configured to programmably increase the rate for decreasing the expiration period.

4. (Original) The system as recited in claim 1, wherein the timing logic unit is arranged within at least one of the source and target devices.

5. (Original) The system as recited in claim 4, further comprising a carrier medium configured to transfer information associated with the transaction cycle between the source device and the target device.

6. (Original) The system as recited in claim 5, wherein the carrier medium comprises one or more buses within a computer system, such that the source and target devices are each arranged within the computer system.

7. (Original) The system as recited in claim 5, wherein the carrier medium comprises a wired or wireless network interface for coupling the system to one or more additional systems, such that the source device is arranged within the system and the target device is arranged within one of the additional systems, or vice versa.

8. (Original) A computer system, comprising:

a source device configured to initiate a transaction cycle by sending a transaction request to a target device;

a timing logic unit arranged within the target device, wherein the timing logic unit comprises:

a time register for storing a predetermined expiration value;

a first counter for receiving a number of pulses corresponding to the predetermined expiration value, and generating a time expired signal upon receipt of a last one of the number of pulses; and

a memory device for storing program instructions configured to programmably alter a rate at which the number of pulses are received by the first counter, thereby adjusting an expiration period for completing the transaction cycle.

9. (Original) The computer system as recited in claim 8, wherein the program instructions are configured to programmably decrease the rate, thereby increasing the expiration period, if a target-ready signal is not asserted by the target device before the time expired signal is generated by the timing logic unit.

10. (Original) The computer system as recited in claim 8, wherein the program instructions are configured to programmably increase the rate, thereby decreasing the expiration period, if a target-ready signal and a source-ready signal are asserted by the target device and the source device, respectively, before the time expired signal is generated by the timing logic unit.

11. (Original) The computer system as recited in claim 9, wherein the target-ready signal is asserted upon completion of the transaction request by the target device, and wherein the source-ready signal is asserted when the source device is ready to send or receive transaction data, which corresponds to the transaction request, for completing the transaction cycle.

12. (Original) The computer system as recited in claim 10, wherein the target-ready signal is asserted upon completion of the transaction request by the target device, and wherein the source-ready signal is asserted when the source device is ready to send or receive transaction data, which corresponds to the transaction request, for completing the transaction cycle.

13. (Original) The computer system as recited in claim 8, further comprising a processor coupled for receiving interrupt signals from a clock source at a fixed rate and for executing the program instructions in response to the interrupt signals.

14. (Original) The computer system as recited in claim 13, wherein the timing logic unit further comprises:

a control register for storing an enable signal;

a second counter for generating the number of pulses; and

a circuit comprising the time register and the first counter, wherein the circuit is coupled to receive the enable signal and at least one of the number of pulses every n^{th} time the processor receives an interrupt signal, wherein 'n' is a programmable value selected from a group consisting of any positive, non-zero integer value.

15. (Original) The computer system as recited in claim 14, further comprising a primary bus bridge logic unit configured to coordinate transactions between the processor, the memory device, and one or more peripheral devices coupled to

the primary bus bridge logic unit over one or more peripheral buses of the computer system.

16. (Original) The computer system as recited in claim 15, wherein the timing logic unit is arranged within the primary bus bridge logic unit.

17. (Original) The computer system as recited in claim 15, wherein the timing logic unit is arranged within the one or more peripheral devices.

18. (Original) The computer system as recited in claim 15, further comprising a secondary bus bridge unit coupled to the primary bus bridge unit over one of the peripheral buses and having one or more additional peripheral devices coupled thereto, wherein the timing logic unit is arranged within the secondary bus bridge unit and/or within the one or more additional peripheral devices.

19.-36. (Canceled).

IX. EVIDENCE APPENDIX

None.

X. RELATED PROCEEDINGS APPENDIX

None.